REMARKS

Claims 1, 3-6, 8-10, 12-15, and 17-27 remain in the application with claims 1, 8, 10, 17, 20, 21, and 25-27 having been amended hereby and claims 7 and 16 having been canceled, without prejudice or disclaimer.

Reconsideration is respectfully requested of the objection to claim 1 as containing informalities.

Claim 1 has been amended hereby to correct the editorial error noted by the Examiner.

Reconsideration is respectfully requested of the rejection of claims 1, 3-7, 10, 12-16, 20, 21, and 25-27 under 35 U.S.C. 102(b), as being anticipated by *Smolansky, et al.*

As previously explained, an exemplary embodiment of the present invention selectively controls a data width of a input/output buffer "on the fly" during memory access operations. Briefly stated, according to an exemplary embodiment of the present invention, an external width control signal is received at an input buffer and a read/write command signal is received at another input buffer. A row address is provided to a decoder along with the read/write command signal. A width control signal is generated in the decoder, and it is sent to an input buffer controller and to an output buffer controller. Depending upon the read/write signal, the input buffer control signal is generated or the output buffer control signal is generated. These buffer control signals are used to control the input/output width of the input buffer and the output buffer.

As noted above, the decoder decodes the external width control signal along with the read and write signals to produce the width control signal fed to the input buffer controller and fed to the output buffer controller, which buffer controllers control their respective buffer memories. As shown in FIG. 7, the decoder includes switches that receive the read/write signal and a plurality of AND gates that decode the external width control signal. Thus, an economical use of circuit elements can provide the data width control without requiring a complex circuit structure.

The claims have been amended hereby to emphasize the above-noted features of the exemplary embodiment of the present invention.

Smolansky, et al. relates to an adjustable width FIFO buffer for variable width data transfers and shows in FIG. 3, for example, a host data FIFO buffer. In this host data FIFO

buffer, an address from an external bus is decoded in an address decoder 102 and fed to both a read control logic 90 and write control logic 98. Signals from a DSP control register and an interface control register are fed to a bus narrow/wide control signal unit that controls the register write and read control logic units. In *Smolansky, et al.*, the details of the address decoder 102 are not provided and it is simply stated that it provides a write enable signal or a read enable signal to the appropriate register read/writer control logic 90 or 98.

In *Smolansky, et al.*, the register read control logic 90 produces a read control signal fed to registers 73 and the register write control logic 98 produces a write control signal fed to registers 75, however, no details of how this is performed are provided. In any event, width control is not provided by the decoder 102, as in the presently claimed invention.

Accordingly, it is respectfully submitted that details of the decoder that decodes the address bits of the external address signal, as taught by the present invention and as recited in the amended claims, are not found therein. Furthermore, *Smolansky, et al.* does not provide any suggestion as to the manner in which this operation should be performed.

All of the amended claims include the specifics of the operation of the decoder, as well as its construction.

Reconsideration is respectfully requested of claims 8, 9, and 17-19 under 35 U.S.C. 103(a), as being unpatentable over *Smolansky, et al.* in view of *Miyata, et al.*.

These claims are dependent claims that depend upon independent claims 1 and 10, respectively, which independent claims are thought to be patentably distinct over the cited references and, for at least those very same reasons, claims 8, 9, and 17-19 are also submitted to be patentably distinct thereover.

Although *Miyata, et al.* relates to a word length selectable memory. *Miyata, et al.* does not cure the deficiencies of *Smolansky, et al.* because *Miyata, et al.* does not provide the details of the decoder that decodes the external address signal, as in the presently claimed invention.

Reconsideration is respectfully requested of the rejection of claims 22-24 under 35 U.S.C. 103(a), as being unpatentable over *Smolansky, et al.* in view of *Hirai*.

These dependent claims depend from independent claim 21 which, for the reasons set forth hereinabove, is thought to be patentably distinct over the cited references and, for at least those very same reasons, claims 22-24 are also submitted to be patentably distinct thereover.

Accordingly, in view of the amendments made to the claims hereby, as well as the above remarks, it is respectfully submitted that a semiconductor memory device and method in which the data width of a data input/output buffer is controlled "on the fly," as taught by the present invention and as recited in the amended claims, is neither shown nor suggested in the cited references, alone or in combination.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
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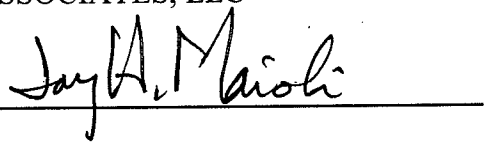

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